DERWENT-ACC-NO: 2001-474408

DERWENT-WEEK: 200151

TITLE: Internal clock generating apparatus for testing
semiconductor device

INVENTOR: BAE, J U; SHIN, J G

PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 1999KR-0031113 (July 29, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001011641 A	February 15, 2001	N/A	001	G11C 029/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001011641A	N/A	1999KR-0031113	July 29, 1999

INT-CL (IPC): G11C029/00

ABSTRACTED-PUB-NO: KR2001011641A

BASIC-ABSTRACT:

NOVELTY - An internal clock generating apparatus is provided to reduce test time by generating internal test clock pulses synchronized with both the rising and falling edges of a source clock signal, respectively.

DETAILED DESCRIPTION - An apparatus comprises an input buffer(10) for taking as an input a source clock signal and converting the external TTL level into CMOS level; a **rising edge detection** unit(20) for detecting the **rising edge** of a source clock signal(clock); a **falling edge detection** unit(30) for detecting the

falling edge of the source clock signal; and an internal clock signal generating unit(40) for outputting an internal test clock signal(iclkp)
synchronized with the **rising edge and the falling edge** of the source clock
signal, respectively, during a high speed operation test **mode** of the semiconductor device.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: INTERNAL CLOCK GENERATE APPARATUS TEST SEMICONDUCTOR DEVICE

DERWENT-CLASS: U11 U14

EPI-CODES: U11-F01C; U14-D01B;